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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of	:	March 5, 2002
H.H. Chen, et al	:	Group Art No.: 2811
Serial No. 09/579,044	:	Examiner: O. Nadav
Filed: May 26, 2000	:	for IBM Corporation Anne Vachon Dougherty 3173 Cedar Road Yorktown Heights, NY 10598
Title: SEMICONDUCTOR HIGH DIELECTRIC CONSTANT DECOUPLING CAPACITOR STRUCTURES AND PROCESS FOR FABRICATION		

PRELIMINARY AMENDMENT

Commissioner for Patents
Washington, D.C. 20231

Sir:

This Preliminary Amendment is being filed simulatneously with the filing of a Continuation in Part Application. The Preliminary Amendment responds to the issues raised in the Final Office Action dated December 5, 2002.

Applicants wish to amend the Patent Application as follows:

IN THE SPECIFICATION:

The newly-submitted Specification includes the new versions of the paragraphs having the following changes, which are detailed on separate pages below.

The paragraph found from page 8, line 17 through page 9, line 17 is replaced with the new version set forth on the attached page.

The paragraph found from page 17, line 12 through page 18, line 14 is replaced with the new version set forth on the attached page.

IN THE DRAWINGS:

The original Figure 5 is replaced with the accompanying new version of Figure 5.

The original Figures 8C through 8K are replaced with the accompanying new versions of Figures 8C through 8K.

IN THE CLAIMS:

Amend Claims 1 and 7 as set forth on the accompanying pages.

MARKED UP VERSION OF PARAGRAPH FROM P.8, L17-P.9,L17

In accordance with the present invention, a high dielectric constant material, which is process-compatible with the semiconductor chip processing, is provided between adjacent metal lines and/or adjacent metal layers on the chip itself. In yet another embodiment, the high dielectric constant material is provided between metal lines and/or between metal layers in a semiconductor packaging structure. The high dielectric constant material is chosen from the group consisting of ferroelectrics, relaxors, paraelectrics, perovskites, pyrochlores, layered perovskites or any material with a dielectric constant which is greater than or equal to 10. Examples of such materials include Ta_2O_5, $BaTiO_3$, $SrTiO_3$, $BaStTiO_3$ (BST or BSTO), $PbZrTiO_3$ (PZT), $PbZrO_3$, $PbLaTiO_3$ (PLT), and $SrBiTiO_3$ (SBT). In addition, any other dielectric material having a dielectric constant which is 2-3 times higher than that of conventional oxide, and which is process-compatible with the semiconductor chip processing (e.g., silicon nitride, aluminum oxide, TiO_2 HfO_2, etc.), can be used. Hereinafter, all eligible materials <u>will be</u> [with be] generically referred to as "high-k" materials.

NEW VERSION OF PARAGRAPH FROM P.8,L17-P.9,L17

In accordance with the present invention, a high dielectric constant material, which is process-compatible with the semiconductor chip processing, is provided between adjacent metal lines and/or adjacent metal layers on the chip itself. In yet another embodiment, the high dielectric constant material is provided between metal lines and/or between metal layers in a semiconductor packaging structure. The high dielectric constant material is chosen from the group consisting of ferroelectrics, relaxors, paraelectrics, perovskites, pyrochlores, layered perovskites or any material with a dielectric constant which is greater than or equal to 10. Examples of such materials include Ta_2O_5, $BaTiO_3$, $SrTiO_3$, $BaStTiO_3$ (BST or BSTO), $PbZrTiO_3$ (PZT), $PbZrO_3$, $PbLaTiO_3$ (PLT), and $SrBiTiO_3$ (SBT). In addition, any other dielectric material having a dielectric constant which is 2-3 times higher than that of conventional oxide, and which is process-compatible with the semiconductor chip processing (e.g., silicon nitride, aluminum oxide, TiO_2 HfO_2, etc.), can be used. Hereinafter, all eligible materials will be generically referred to as "high-k" materials.

MARKED UP VERSION OF PARAGRAPH FROM P.17, L12-P.18, L14

To process further, a higher level of interconnect with a similar high-k material capacitor is formed. The process comprises first forming metal contact 815 with conductive adhesion liner 817 in second dielectric layer 812 as shown in Figure 8G. The metal contact [8159] 815 can be formed by Damascene processing such as is used to form metal wires. The second dielectric layer is patterned, for example by depositing a photoresist and etching an opening in the dielectric using a selective etch, as was described with reference to layer 802 above. Once the opening in the dielectric layer 812 has been defined, an electrically conductive diffusion material 827 is deposited on the top of the structure as shown in Fig. 8H. High-k material 819 is conformally deposited over the electrically conductive diffusion barrier layer 827 as shown in Fig. 8I. Thereafter, the high-k material is polished back to the electrically conductive diffusion barrier, as shown in Fig. 8J, followed by etching of the electrically conductive diffusion barrier layer 827. Another diffusion barrier metal 837 is deposited, followed by formation of a top metal wire 833 by metal etching

using a photoresist as a mask to first etch the metal and then remove the exposed diffusion barrier layer 837. The resulting cross-sectional view is shown in Fig. 8K. The high-k material 819 is sandwiched between two metal lines 805 and 833, thereby forming the vertical decoupling capacitor.

NEW VERSION OF PARAGRAPH FROM P.17, L12-P.18, L14

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and then remove the exposed diffusion barrier layer 837. The resulting cross-sectional view is shown in Fig. 8K. The high-k material 819 is sandwiched between two metal lines 805 and 833, thereby forming the vertical decoupling capacitor.

MARKED-UP VERSION OF AMENDED CLAIMS

1. (Amended) A semiconductor structure comprising:

a substrate;

two or more adjacent conductors, disposed in at least one dielectric layer formed over said substrate and electrically isolated from each other, wherein each pair of adjacent conductors is separated by a gap; and

a first high dielectric constant material formed in the gap between two adjacent conductors.

7. (Amended) The semiconductor structure of Claim 1 wherein at least one pair of adjacent conductors comprises a power supply line [an] and a ground wire.

NEW VERSION OF CLAIMS WITH INCORPORATED AMENDMENTS

1. A semiconductor structure comprising:

a substrate;

two or more adjacent conductors, disposed in at least one dielectric layer formed over said substrate and electrically isolated from each other, wherein each pair of adjacent conductors is separated by a gap; and

a first high dielectric constant material formed in the gap between two adjacent conductors.

7. The semiconductor structure of Claim 1 wherein at least one pair of adjacent conductors comprises a power supply line and a ground wire.

REMARKS

In the Final Office Action, the Examiner indicated that the corrected drawings introduced new matter. To avoid the rejection, Applicants are filing a CIP application to introduce the corrected drawings and text into the patent application. While Applicants asserted that no new matter was added to the application by the submission of new versions of the figures, since the originally-filed application detailed the illustrated embodiment in the text which accompanied the figures in the original Specification (see, e.g., page 12, line 5 through page 13, line 4), as well as in Claims 10 and 11, Applicants are nonetheless filing the CIP. The changes to Figure 5 include correction of the reference numeral 529 to 519 as well as correction of the illustration of the diffusion barrier to be consistent with the description and claims.

The Examiner had additionally objected to the Specification due to informalities resulting from two typographical errors, one each on pages 8 and 17. Each of the errors have been corrected by the replacement of the paragraphs in which the errors occurred. Applicants believe that the objections are addressed by the amendments submitted herein and assert that no new matter is added by the amendments to the Specification.

Claim 7 had been rejected under 35 USC 112 as indefinite due to the typographical error found therein. As was clear from the Specification (see, e.g., page 13, lines 10-13), the claim recited the embodiment wherein the adjacent conductors comprise a power supply **and** a ground wire. A new version of Claim 7 has been provided by this amendment.

With regard to the rejections of the claims as unpatentable over the teachings of the Geffken, et al patent, alone and in combination with the teachings of the Lee patent. The Geffken patent teaches a structure in which decoupling capacitors are provided with increased surface area (and therefore increased capacitance) by including both the top surface of embedded metal plugs 12 as well as the side and top surfaces of metal studs 14 as the first capacitor plate. The Examiner has referenced "...two or more adjacent aluminum conductors 14' disposed in at least one dielectric layer 28...{and} ...separated by a gap, and first high dielectric constant material 18' formed in the gap between two adjacent conductors...". Applicants note that material 18' is not a dielectric material but is a conductive layer (see: Col.. 3, lines 20-21. Furthermore, each pair of conductors 14' in the Geffken patent is electrically connected to each other (see: the overlap of the bottom surface of stud 14' and the top surface of the embedded metal plug 12' which provides electrical connection of all of the conductors). Clearly no

capacitance is being realized between electrically connected studs 14'. The capacitors of Geffken are comprised of first metal "plate" 12',14', intermediate dielectric layer 16', and second metal "plate" 18'. The structure of Geffken does not anticipate the invention as claimed.

To further highlight the differences between the Geffken structure and the present invention, the language of independent Claim 1 has been amended to emphasize that the two adjacent conductors are electrically isolated from each other, as is clearly taught and illustrated by the present application, and which is clearly not taught or suggested by the Geffken patent.

With regard to the Examiner's comments regarding Claims 9 and 10, Applicants note that the Geffken patent provides for electrical connection between the top "plate" 18' and the next level of metal (interconnect stud 20 and studs 22), so that no capacitance can be built up between the "plates" of such a vertically arranged capacitor. Applicants, on the other hand, expressly teach and illustrate lateral as well as vertical capacitor structures wherein the adjacent and/or successive metal structures are electrically isolated from each other with the high dielectric constant material(s) disposed therebetween, to thereby form one or more capacitors. Geffken clearly does not teach electrically isolated metal structures as is taught and claimed by the present invention.

Regarding the Examiner's comments in rejecting Claim 12, Applicants again disagree with the Examiner's description of what the Geffken patent teaches and illustrates. In Figure 2 of Geffken, the material 26 is not disposed between a second high dielectric constant material 24 and the conductor 22. Rather, what Geffken illustrates is a high dielectric constant material 24 between metal 22 and conductive material 26.

As to the Examiner's comments in rejecting Claim 13, the Examiner again states that the electrically conductive barrier material 26 is disposed between high dielectric constant material 24 and conductor 22. As illustrated in Geffken's Figure 2, however, layers 24 and 26 are continuous over the studs 22 and are not, therefore, disposed between them. Furthermore, Geffken's Figure 2 shows a further unfilled gap between the electrically connected conductor studs 22. Again, Applicants fail to see how the illustrated Geffken structure obviates the invention as claimed.

The Examiner has also rejected Claims 3, 7, and 14 as unpatentable over the combination of teachings of the Geffken and Lee patents. As discussed above, the Geffken patent has not been properly interpreted in rejecting Claims 1-2, 4-6, and 8-13. Furthermore, Applicants respectfully contend that the Lee patent does not provide those teachings which are missing from the Geffken patent for rejecting the independent claim, Claim 1, or any of the remaining claims which depend therefrom. While the

Lee patent discloses the use of a high dielectric constant material in a capacitor, such does not obviate the claimed structure wherein a high dielectric material is disposed between adjacent conductors which are electrically isolated from each other and/or between successive layers of conductors which are electrically isolated from each other, let alone such structures further comprised of specific materials and/or dimensions.

Applicants assert that even if one were to combine the teachings of the Geffken and Lee patents, one would not arrive at the invention as claimed. If one having skill in the art were to modify Geffken using the Lee teachings, one would arrive at the Geffken structure, having electrically connected metal studs as a first capacitor plate (e.g., 12' and 14' of Figure 2), the Lee high dielectric material as the intermediate capacitor dielectric (layer 16'), and conductive material 18' as the second capacitor plate. Such a combination would not obviate the invention as claimed. Accordingly, Applicants believe that the pending claims are patentable over the cited combination of references and respectfully request withdrawal of the rejections under 35 U.S.C. 103.

Based on the foregoing amendments and remarks, Applicants respectfully request entry of the amendments, withdrawal of the objections, withdrawal of the rejections, and issuance of the claims.

Respectfully submitted,

H.H. Chen, et al

By: ____________________

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